REMARKS

This Amendment is in full and timely reply to the Office Action mailed November 7, 2006. The applicant notes with appreciation that receipt of priority documents and consideration of the Information Disclosure Statement submitted June 2, 2004 have been acknowledged by the examiner.

Drawings

Figs. 9 and 10 have been amended to include the legend "PRIOR ART" as requested in the November 7 Office action. Additionally, Fig. 9 has been amended to correct slight drafting errors. No new matter has been added by these amendments.

Claims

The Applicant's original claims 1-4, 7-9, and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,670,944 to Ishii ("Ishii") in view of U.S. Pat. No. 5,886,353 to Spivey et al. ("Spivey"). This rejection is traversed.

Ishii describes a "data line driving circuit" for driving an electro-optical device (such as an LCD). (Ishii, Abstract). Through the addition of several stages of circuitry (e.g., level shifter **1510**, SR latch **1530**, and NAND circuit **1580**) Ishii claims to provide a reduction in power consumption by only providing a high-voltage clock signal to select parts of the circuit at a time. (Ishii, Abstract and 2:33-51, 3:13-23).

Spivey teaches an imaging device for producing images using electron-hole producing radiation. (Spivey, Abstract). As a component of this device, Spivey teaches using shift registers for column and row selection. (Spivey, at 4:61-64 and Fig. 6).

The Applicant's specification describes an improved shift register, utilizing a *reduced* number of transistors between positive and negative power supplies, reducing the required voltages and accelerating the shift register's operation. (Applicant's specification, Abstract, paragraphs 0013, 0044-0045, and Figs. 1, 3, and 5). This reduction is achieved by substituting a NAND circuit within the shift register, rather than the clocked inverters used in the prior art. (Applicant's specification, 0034).

Neither reference individually, nor their combination, teaches or suggests all of the features of the Applicant's invention. For example, with regard to the Applicant's claim 1, neither reference teaches or suggests "[a] shift register including of a plurality of unit circuits each having . . . a time-shifter comprising a NAND circuit to receive an input pulse as one input thereof." Ishii may teach a circuit identified as a "shifter," but this does not satisfy the recited limitations of the Applicant's claim. For example, the shifters (**1510** and **1520**) of Ishii are *level* shifters, not time-shifters. (Ishii, at 11:32-54). These circuits, according to Ishii, shift a low-voltage-swing clock signal into a high-voltage-swing clock signal. (See Ishii, at 12:49-13:67, 14:21-30 and Fig. 5). As can be seen in Figure 8, the outputs of the level shifters (**C0-C4**) are synchronized and in phase with either **CLX** (for $\mathbf{CN_{even}}$) or $\mathbf{CLX_{INV}}$ (for $\mathbf{CN_{odd}}$). Contrast this with Figs. 2, 4 and 6 in the Applicant's specification, depicting the output pulses of the shifters (**A**, **A1**, and **A2**) as extending for one-quarter clock period beyond the end of the input pulse (**st**, **st1**, and **st2**, respectively).

Furthermore, the shifters in Ishii do not comprise NAND circuits. The NAND circuits cited by the Examiner (**1580** and **1590**) are neither components of the shifters nor components of the shift register. Rather, these NAND circuits operate on the *output* of the shift register to constrain its pulse-width. (Ishii, at 12:31-46, 15:58-65). Possibly more analogous elements to the Applicant's time-shifter circuits can be found in Fig. 7 of Ishii. However, these circuits are akin to the prior art show in Applicant's Fig. 9, composed of inverters and clocked inverters, not NAND circuits as recited in the Applicant's claim. Similarly, a possibly analogous circuit in Spivey (**44**) contains inverters and clocked buffers, but no NAND structures. (Spivey, Fig. 7).

Additionally, neither reference teaches [a] shift register including of a plurality of unit circuits each having . . . a holder having a PMOS transistor and an NMOS transistor, which are connected in series between a power supply and a clock input end fed with a clock pulse and of which gates and drains are mutually connected in common respectively, wherein the input end of said holder is connected to the output end of said NAND circuit, and the output potential thereof is fed as another input to said NAND circuit. For example, none of the circuitry in Ishii has the input end connected to the output end of said NAND circuit, and the output fed as another input to said NAND circuit. As shown in the Applicant's Fig. 1, this recited limitation creates a

feedback loop between the holder and the NAND circuit. The NAND circuits in Ishii, by contrast, are not involved in any such loop. (Ishii, Fig. 4). Their output is used to create sampling signals **Sn**, which are not fed back to any of the other circuit elements in data line driving circuit **150**, including those cited by the Examiner. The input end of the phase expansion circuit **302** is the input video signal itself. (Ishii, at 8:7-19). The output of the phase expansion circuit is not an input to the NAND circuit; rather it is controlled through transistor **141**, which is connected to the *output* of the NAND circuit. (Ishii, Fig. 1). The shift register circuits comprised of inverters **1562**, **1564**, and **1566** may output their result (**Sn'**)as an input to the NAND circuits, (Ishii, 14:2-20, 15:58-65), however the output of the NAND circuits are not connected to the input of the shift register circuits and no loop is described.

Furthermore, Ishii does not address the connection of individual transistors at all. Merely reciting that the **NAND circuits** "are formed of p-channel TFTs or a combination of p-channel and n-channel TFTs" does not suggest that the **holder** specifically has a PMOS transistor and an NMOS transistor connected, in the specific recited manner, between the power supply, the clock signal, and the output of the NAND circuit. As previously stated, the stages of the shift register **1560** cannot be interpreted to suggest the recited limitations, as they do not receive input from the outputs of the NAND circuits, nor are they (or their component individual transistors) shown as being connected in series between a power supply and a clock input.

The "sample and hold" circuitry taught in Spivey (**54**) is in no way related to the shift registers **32**, **36** or their component parts **44**. (Spivey, Fig. 6). The sample and hold circuits of Spivey serve to store the analog voltage level read from a given pixel. (Spivey, at 5:43-52, 6:40-57 and Fig. 8A). Similar to the circuitry in Ishii, this sample and hold circuit does not satisfy the recited transistor types or connection requirements of the Applicant's claim, nor is it involved in any type of feedback loop to affect the input pulse of the shift register.

In summary, the while Ishii may teach shifters and NAND circuits, and Spivey may teach sample-and-hold circuits, none of these elements are being used in a similar fashion to what is recited in Applicant's claim 1, nor does any satisfy the specific connection limitations recited. Therefore the Applicant's claim 1 is patentable over these references for at least these reasons. For at least reasons similar to these, Applicant's claim 7, directed to a display device having a

shift register with similar limitations to those in claim 1, is also patentable over these references. Furthermore, claims 2-6 and 8-12, being dependent on claims 1 and 7, respectively, and incorporating all of their limitations, are also patentable over these references.

With regard to the Applicant's claim 2, neither reference teaches or suggests odd-stage unit circuits and [] even-stage unit circuits [that] operate in synchronism respectively with clock pulses having a 1/4 phase difference from each other. For example, Ishii teaches that alternating stages of the shift register utilize clock pulses that are respectively *inverted* (**CLX** and $\mathbf{CLX}_{INV}$). (Ishii, at 11:32-61, Figs. 8, 11, and 13). At best, these clock signals can be said to have a 1/2 phase difference. Compare these with clock signals **ck1** and **ck2** shown in Applicant's Fig. 4, depicting two clock signals with a 1/4 phase difference. The passage cited by the Examiner (Ishii, 8:6-40) describes the phase expansion circuit, which extends the duration of the video signal to N-phases (N=6). This video signal is never used as input into the driving cirtuit. (Ishii, Fig. 1). Whether the value of N is arbitrary and could indeed be 4 has no bearing on the relative phase difference of the *clock* pulses sent to stages of the shift register. As described by Ishii, whether N is 1, 2, 4, or 6, the relative phase difference of the clock pulses is still 1/2.

Therefore the Applicant's claim 2 is patentable over these references for at least these reasons. For at least reasons similar to these, Applicant's claim 7, directed to a display device having similar clock-phase limitations to those in claim 2, is also patentable over these references. Furthermore, claims 8-12, being dependent on claim 7 and incorporating all of its limitations, are also patentable over these references.

Furthermore, the Examiner has used improper rationale to combine these references. The use of CMOS fabrication techniques is extremely well-known in the art as a method for improving response time and reducing power consumption. A search for "CMOS" in the specifications of patents issued from 1976 yields over 69,000 results. Thus one of skill in the art would not be guided to select Spivey in combination with Ishii merely to gain the advantages of CMOS technology. This type of rationale is akin to an erroneous "obvious to try" standard. The art has provided numerous possible choices (over 69,000) of implementations of CMOS

technology without suggesting that Spivey in particular would be a desirable selection. *See* MPEP § 2145(X)(B). Furthermore, Ishii already makes reference to transistors of both n- and p-channel types, the essence of CMOS technology. (Ishii, at 12:34-37). Therefore one would not be motivated to look to other references to incorporate CMOS technology with the teachings of Ishii.

The Applicant's original claims 5, 6, 10, and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishii in view of Spivey and in further view of U.S. Pat. No. 6,930,665 to Sekine ("Sekine"). This rejection is traversed.

As detailed above, the combination of Ishii and Spivey fails to teach or suggest the features of Applicant's claim 1. Furthermore, the addition of Sekine does not teach the additional features recited in the applicant's dependent claims. For example, with regard to claim 5, none of these references teach a waveform shaping shift circuit, which shapes the waveform of the input pulse in synchronism with the clock pulse having a 1/4 phase difference from the clock pulse fed to said holder, and then feeds the waveform-shaped pulse to said shifter. Similar to the functionality of the NAND circuit in Ishii, the gate drivers $\mathbf{41_1}$ and $\mathbf{41_2}$ of Sekine modify the signal sent to the pixel array. Sekine, at 12:4-22 and Figs. 21-24, 26). This modified waveform is never fed to the shifter as recited in the Applicant's claim.

Therefore the Applicant's claim 5 is patentable over these references for at least this reason. Furthermore, Applicant's claim 10, directed to a display device having a similar waveform shaping shift circuit, is also patentable over these references. Additionally, claims 6 and 11, being dependent on claims 5 and 10, respectively, and incorporating all of their limitations, are also patentable over these references.

Additionally, with regard to the Applicant's claim 6, none of these references teach an inverter circuit for inverting the phase of said input pulse and feeding the phase-inverted pulse to said waveform shaping shift circuit. The inversion referred to in Ishii at col. 8, lines 20-31 is an inversion of the video signal, not of the input pulse **DX**. The video signal is never used as input into the shift register; rather it is input to the pixel array. (Ishii, Fig. 1).

Therefore the Applicant's claim 6 is patentable over these references for at least this reason. Furthermore, Applicant's claim 11, directed to a display device having a similar inverter circuit, is also patentable over these references.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-0013, under Order No. SON-2921 from which the undersigned is authorized to draw.

Dated: April 4, 2007

Respectfully submitted,

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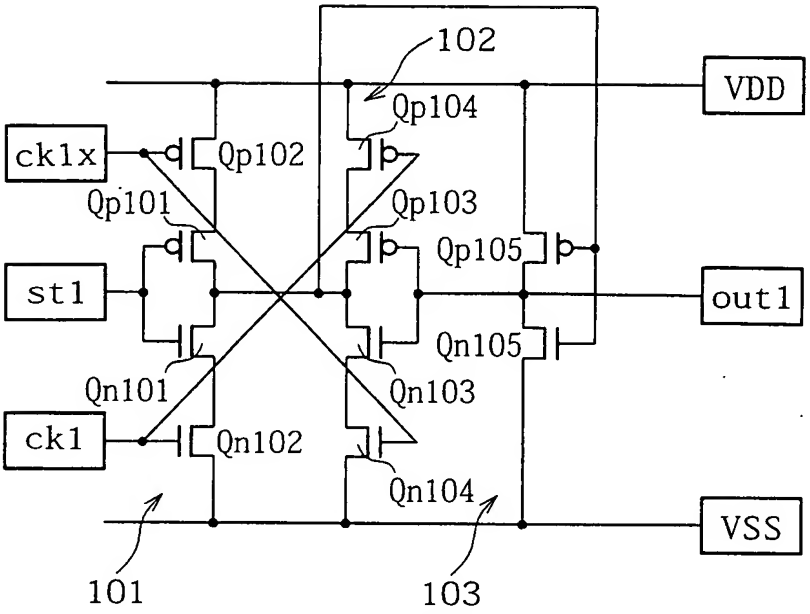
Attachments: Amendment Transmittal
Petition for Extension of Time (two months)
Annotated Sheet of Drawing Figs. 9 & 10
Replacement Sheet of Drawing Figs. 9 & 10

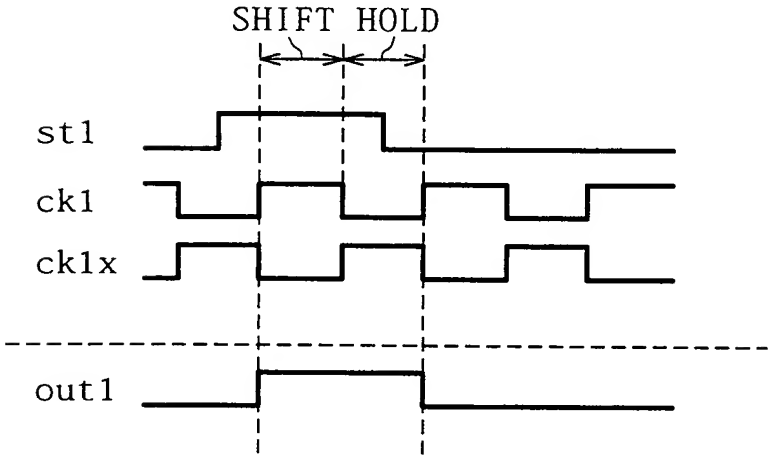
(Annotated Sheet)

FIG. 9



PRIOR ART

FIG. 10



PRIOR ART